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Low Power VLSI Design of SPST Analog Switch

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Abstract—This paper represents a single pole single through (SPST) analog switch designed using VLSI. An SPST switch has a single pole and can connect only one line to other network. The switching performance depends on the switching time and power dissipation in it. This study is done to design a new SPST switch that dissipates very low power and the switching time is also very low. At first the layout of the switch has been developed whose output is then fed to a refresh circuit. The refresh circuit is used to reshape the signal as it distorted due to switching effect. The output of the refresh circuit is found both in inverted and non-inverted form. A pad frame is designed in which the original circuit is imported to make a 10 pin integrated circuit (IC).

Index Terms—SPST, VLSI, power dissipation, refresh circuit, layout, pad frame.

1 INTRODUCTION

IN electronics, a switch is an electrical component that can break an electrical circuit, interrupting the current or diverting it from one conductor to another [1]. The most familiar form of switch is a manually operated electromechanical device with one or more sets of electrical contacts. Each set of contacts can be in one of two states: either 'closed' meaning the contacts are touching and electricity can flow between them, or 'open', meaning the contacts are separated and nonconducting.

A switch may be directly manipulated by a human as a control signal to a system, such as a computer keyboard button, or to control power flow in a circuit, such as a light switch [2]. Automatically-operated switches can be used to control the motions of machines, for example, to indicate that a garage door has reached its full open position or that a machine tool is in a position to accept another workpiece. Switches may be operated by process variables such as pressure, temperature, flow, current, voltage, and force, acting as sensors in a process and used to automatically control a system.

SPST (Single Pole Single Throw) is a simple on-off switch: The two terminals are either connected together or disconnected from each other. When the two terminals are connected the input signal is passed to the output terminal. The diode, BJT or MOSFETs can be used as the SPST switch. But the problems of the diode and BJT switches are that they are slow in operation and dissipate higher power [3], [4]. A single MOSFET can be a solution to this problem. But other problem arises from it. The output is lost by an amount of threshold voltage [6]. So, if these switches are cascaded, then the logic level is lost after some stages. To solve this, a pass gate is used. The pass gate can be implemented using diode logic and transistor logic [5], but if offers slower operation and higher power dissipation. So, the SPST switch is implemented with CMOS technology. It can be used to simplify digital logic circuits or to switch analog signals, and so is also known as an analog switch. It is made by the parallel combination of an nMOS and a pMOS transistor with the input at the gate of one transistor being complementary to the input at the gate of the other. It would seem that a transmission gate could be constructed using simply a single pMOS or nMOS transistor. If only an individual nMOS transistor were to be used, and there was a high voltage on the OUT and a low voltage on the IN and it is tried to transmit the zero to the OUT, then the nMOS will drain some of the voltage but not all of it leaving the OUT somewhere in the "no man's land" voltage region of digital circuits. Adding the pMOS gate in parallel allows all the voltage to drain after the nMOS shuts off before all the voltage is drained. This also solves the problem when transmitting a high voltage to OUT [6], [7].Althought the voltage level is recovered; the thermal noise distorts the signals [8]. To remove the distortion of the output signal a refresh circuit has been used to implement a full SPST switch.

2 DESIGN METHODOLOGY

The circuit diagram using only one pass gate and an inverter is shown in the fig. 1. When Control is HIGH both NMOS and PMOS is ON, and the input is passed to the output terminal. Otherwise, both the MOSFETs are OFF and the input and output terminals are disconnected.

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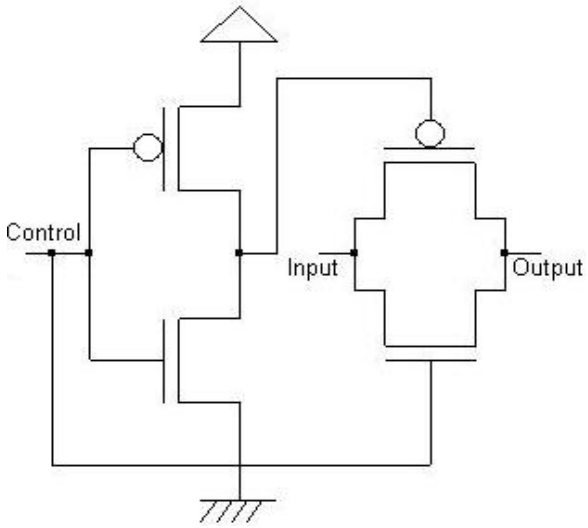

Fig. 1. SPST switch without refresh circuit

To remove the distension from the output signal a refresh circuit is added at the output of the above circuit. The new circuit is shown in fig. 2.

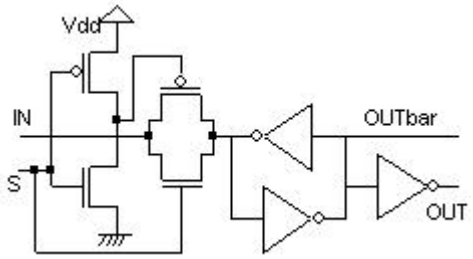

Fig. 2. SPST circuit with refresh circuit

The basic cell or unit cell is designed using the pass transistors. The pass transistors are used so that both the logic level can pass accurately and fully. The layout diagram of a unit cell is shown in the fig. 3. The rules of layout diagram are maintained to provide the device with minimum area [9-11].

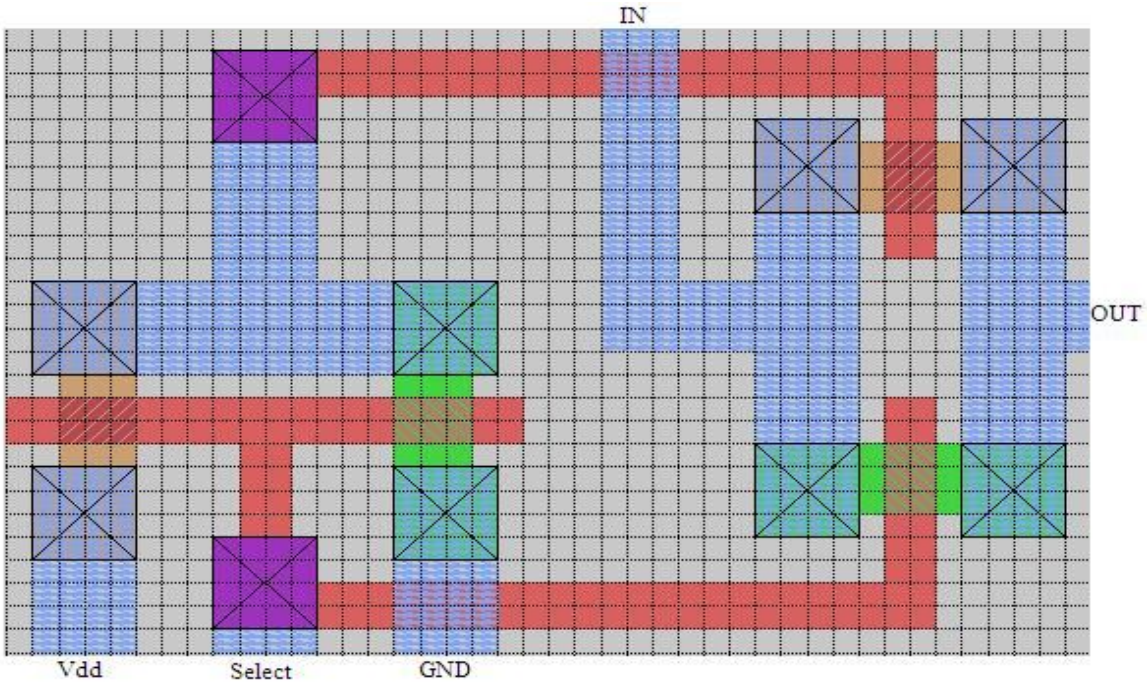

Fig. 3. Layout of the SPST switch without refresh circuit

The output of the cell may be affected by thermal noise in the device. That is why a refresher circuit is cascaded at the output end of the above figure. Thus the diagram of unit cell is replaced by following unit cell in figure2. In this method the output is found both in inverted and non-inverted form. OUT is in inverted form and INVOUT is in inverted form.

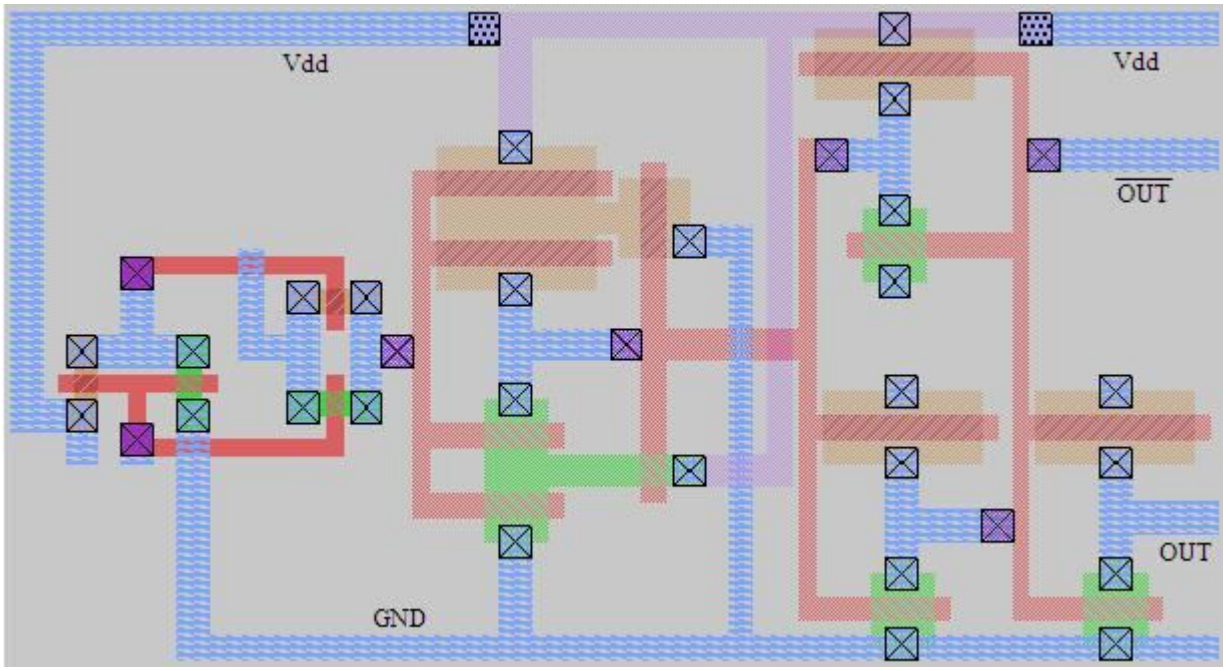

Fig. 4. Layout of the SPST switch with refresh circuit

Now an array is created of the unit cell of figure2 to make a 10 pin SPST switch that includes two switches. The final form of the switch is shown in the figure3. In the figure below: pin_1, pin_2, pin_3 and pin_4 are involved with first switch and pin_6, pin_7, pin_8, and pin_9 are related to second switch. For both of the switches, first pin is the controller of the switch, second pin is the input, third pin is the output in non-inverted form, and the fourth pin is the output in inverted form. Pin_10 is Vdd supply and pin_5 is ground.

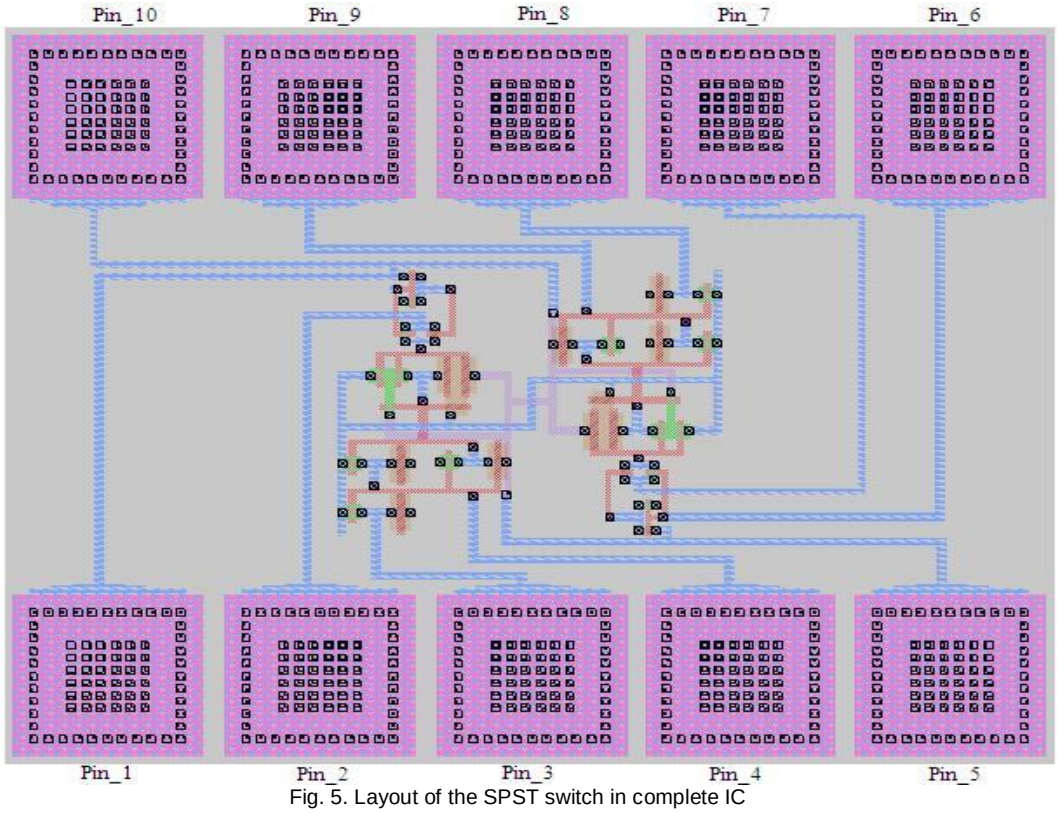

Fig. 5. Layout of the SPST switch in complete IC

3 RESULT

The spice code was extracted from the layout diagram as did in the Magic software [12]. The MOS device parameter was collected from the MOSIS [13]. After combining the extracted code and the device parameter, a simulation was performed in the PSPICE software. The dynamic power dissipation is 0.00251nW which is very low. The ON resistance is very low, both of ON time and OFF time is also very low. A comparison between the switches available in the market with this designed switch is shown in table 1.

TABLE 1

A COMPARISON AMONG SPST SWITCHES

Device Name	Ron (Ω)	Ton (ns)	Toff (ns)
MAX4621	5	250	200
MAX4601	2.5	250	350
MAX4609	2.5	110	150
TS3A4742	.9	14	9
This Work	1	10	7

The SPST switch passes the input to the output terminal by switching action. When the switch is ON the input is followed by the. Figure3 shows this condition. The input is taken as a pulse wave and the switch is controlled by another pulse wave. The output in this figure is shown direct from the basic unit cell. The output is distorted as shown in figure.

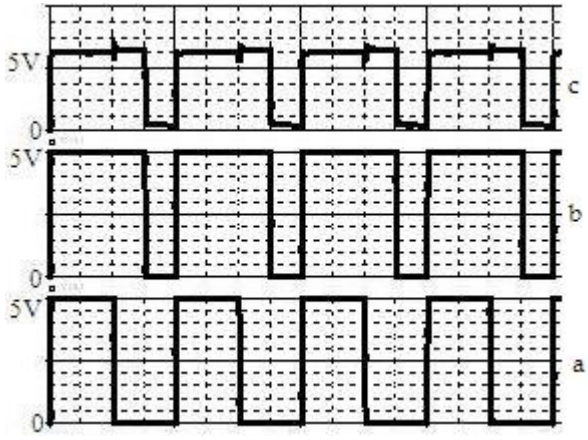

Fig. 6. a) Control b) input c) output without refresh circuit

Now the output is passed through the refresh circuit. Figure4 shows that if the output passes through the refresh circuit, the distorted output is refreshed to follow the actual input. Both the inverted and non-inverted form of the output is shown in the figure below.

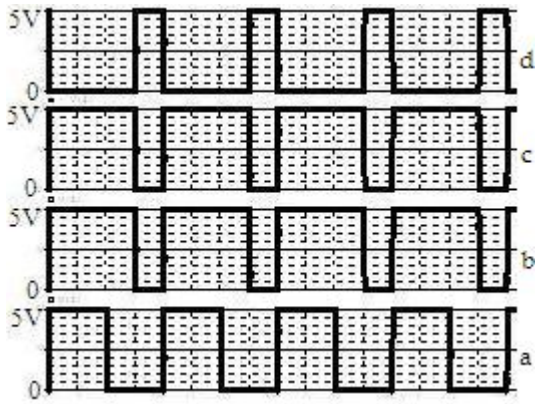

Fig. 7. a) Contorl b) input c) non-inverted output with refresh circuit d) inverted output with refresh circuit

4 CONCLUSION

The goal of this paper was to design a SPST switch and to minimize the power dissipation through it. The designed switch works properly as described in result analysis and the power dissipation is 0.00251nW which is very low. The design can be certified to be correct, because all the design rules were maintained and there was no DRC (Design Rule Check) error found. It also works very fast. The switch can be applied to power routing, audio/video signal routind, communication circuits, modems etc. Further analysis can be done to reduce the power more and more.

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